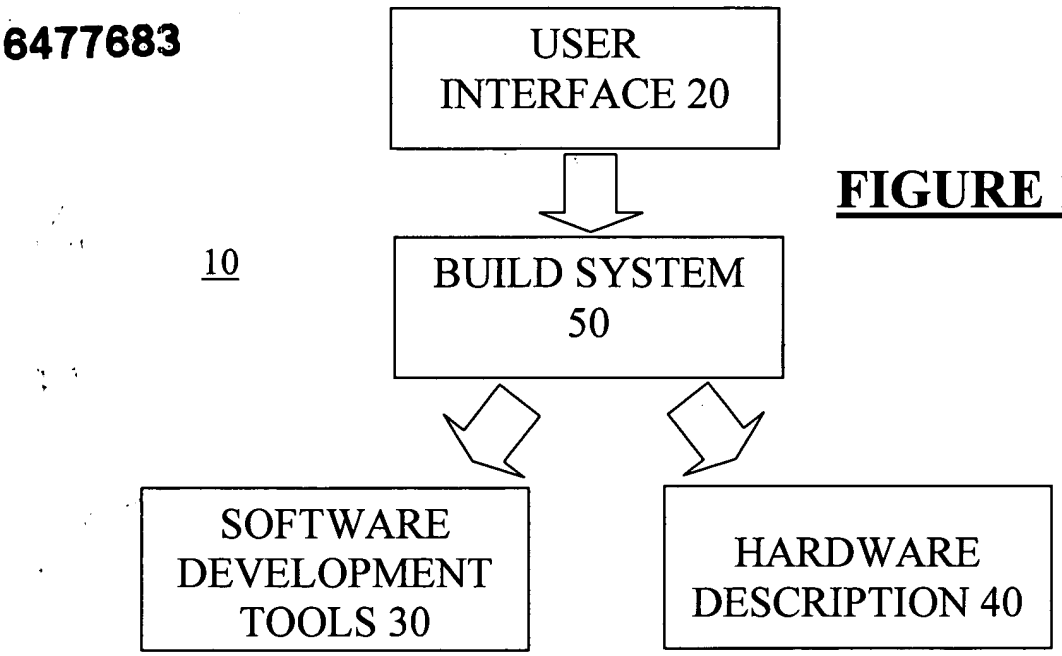

FIGURE 1

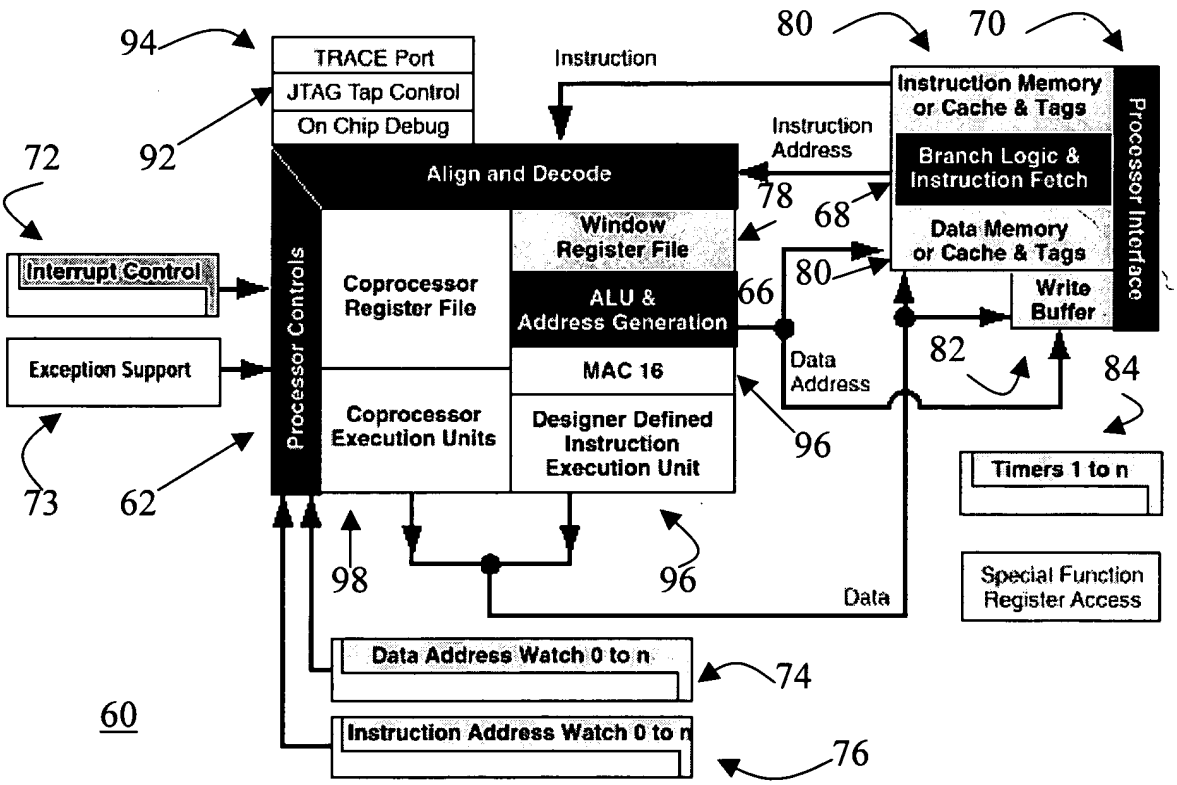

FIGURE 2

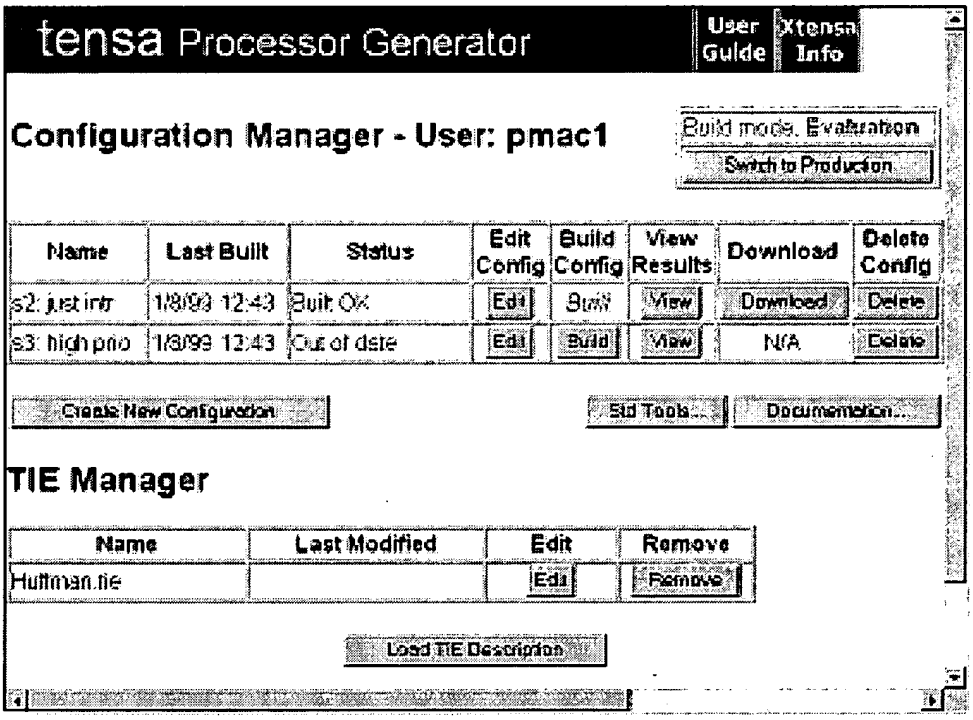

FIGURE 3 86

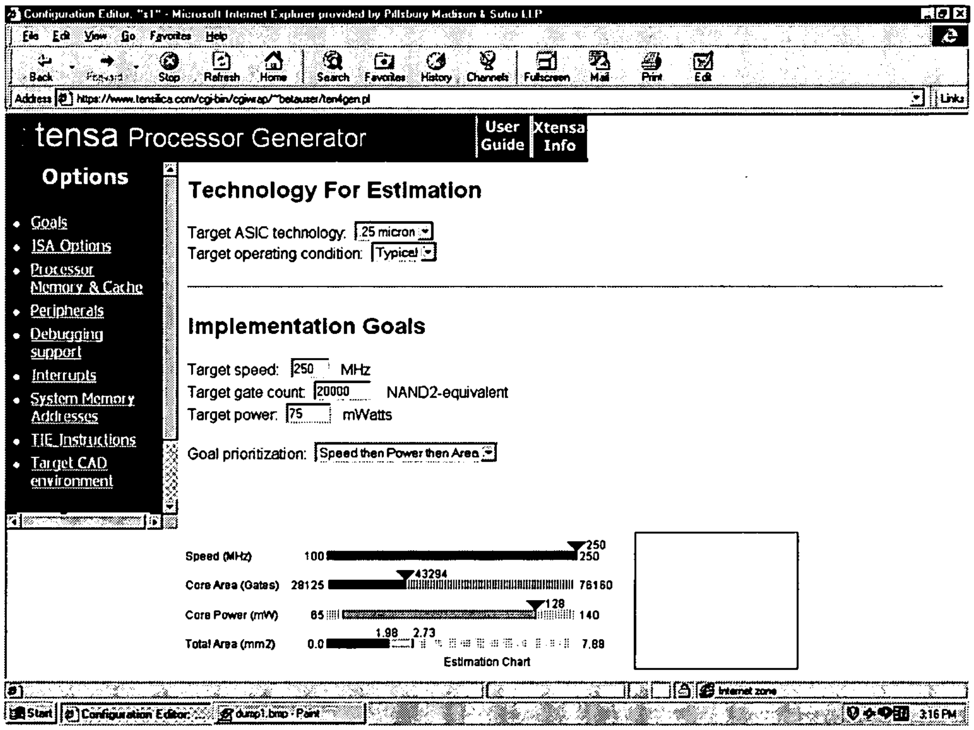
tensa Processor Generator
User Guide
Xtensa Info
Options
Goals
ISA Options
Processor Memory & Cache
Peripherals
Debugging support
Interrupts
System Memory Addresses
TIE Instructions
Target CAD environment
Technology For Estimation
Target ASIC technology: .25 micron
Target operating condition: Typical
Implementation Goals
Target speed: 250 MHz
Target gate count: 20000 NAND2-equivalent
Target power: 75 mWatts
Goal prioritization: Speed then Power then Area
Speed (MHz) 100 250 250
Core Area (Gates) 28125 43294 76160
Core Power (mW) 65 128 140
Total Area (mm2) 0.0 1.98 2.73 7.89
Estimation Chart

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FIGURE 4

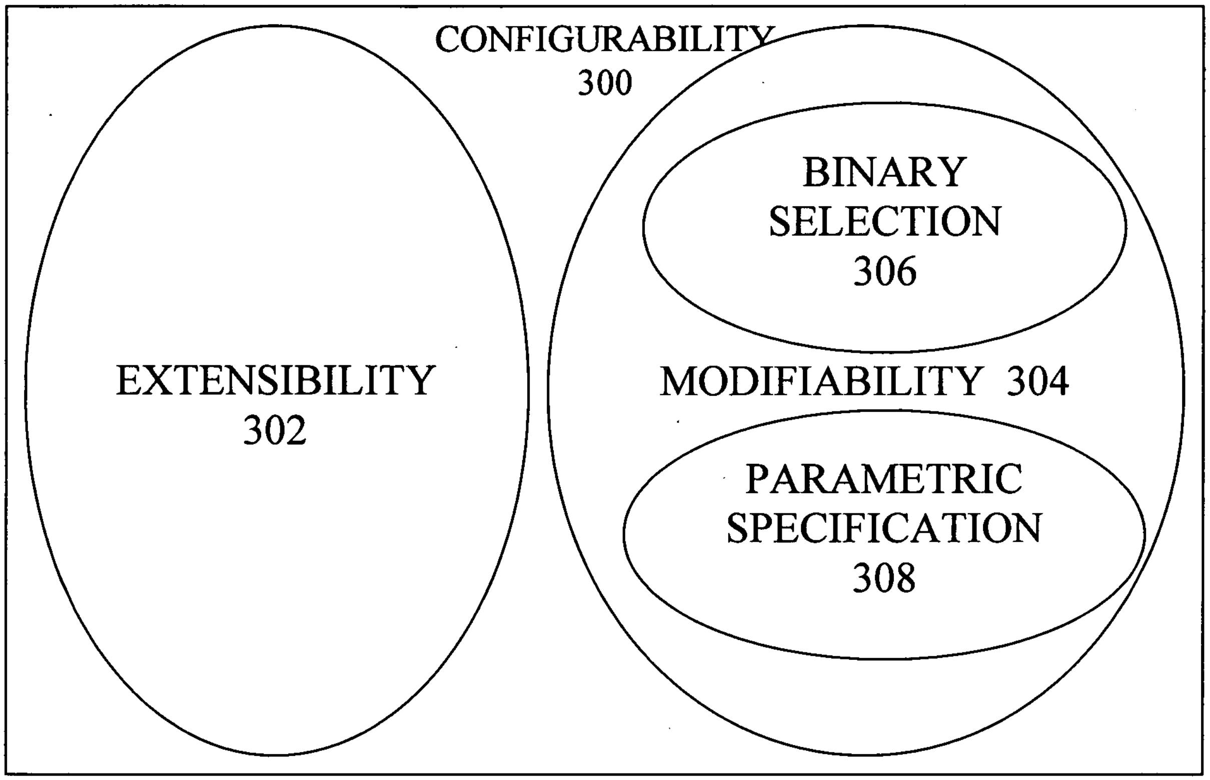

CONFIGURABILITY
300
EXTENSIBILITY
302
BINARY
SELECTION
306
MODIFIABILITY 304
PARAMETRIC
SPECIFICATION
308

FIGURE 5

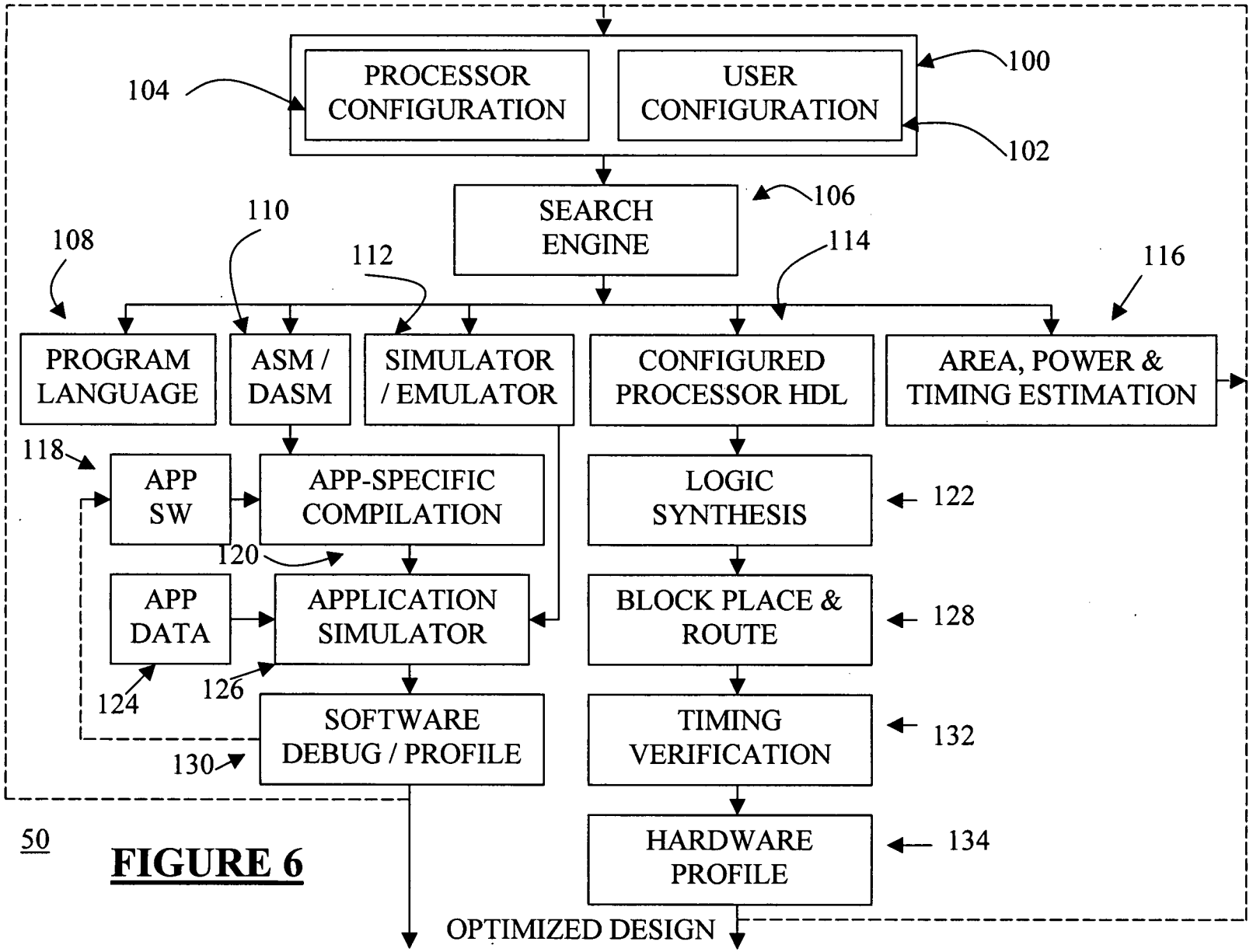
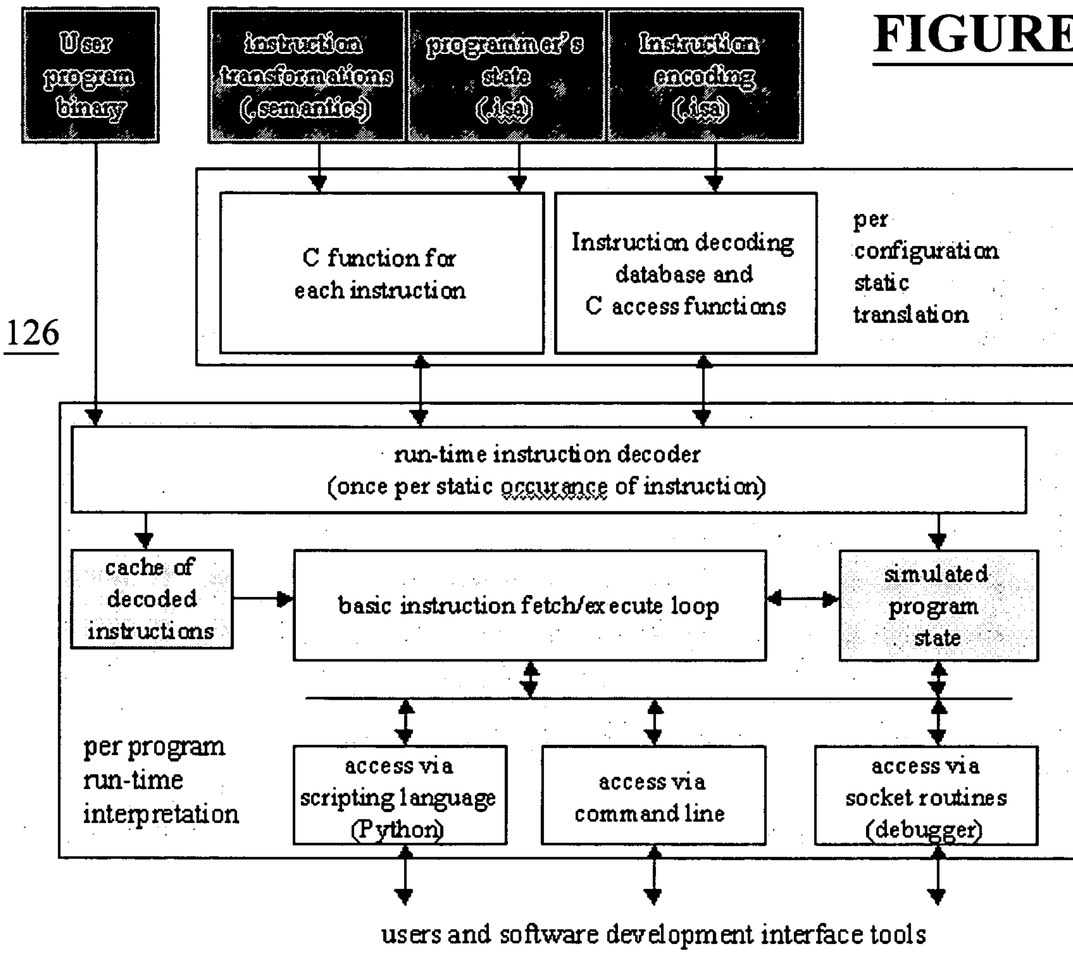

PROCESSOR CONFIGURATION
USER CONFIGURATION
100
102
104
SEARCH ENGINE
106
108
110
112
114
116
PROGRAM LANGUAGE
ASM / DASM
SIMULATOR / EMULATOR
CONFIGURED PROCESSOR HDL
AREA, POWER & TIMING ESTIMATION
118
APP SW
APP-SPECIFIC COMPILATION
LOGIC SYNTHESIS
122
120
APP DATA
APPLICATION SIMULATOR
BLOCK PLACE & ROUTE
128
124
126
SOFTWARE DEBUG / PROFILE
TIMING VERIFICATION
132
130
HARDWARE PROFILE
134
50
OPTIMIZED DESIGN

FIGURE 6

FIGURE 7

126


User program binary
instruction transformations (.semantics)
programmer's state (.isa)
Instruction encoding (.isa)
C function for each instruction
Instruction decoding database and C access functions
per configuration static translation
run-time instruction decoder
(once per static occurance of instruction)
cache of decoded instructions
basic instruction fetch/execute loop
simulated program state
per program run-time interpretation
access via scripting language (Python)
access via command line
access via socket routines (debugger)
users and software development interface tools

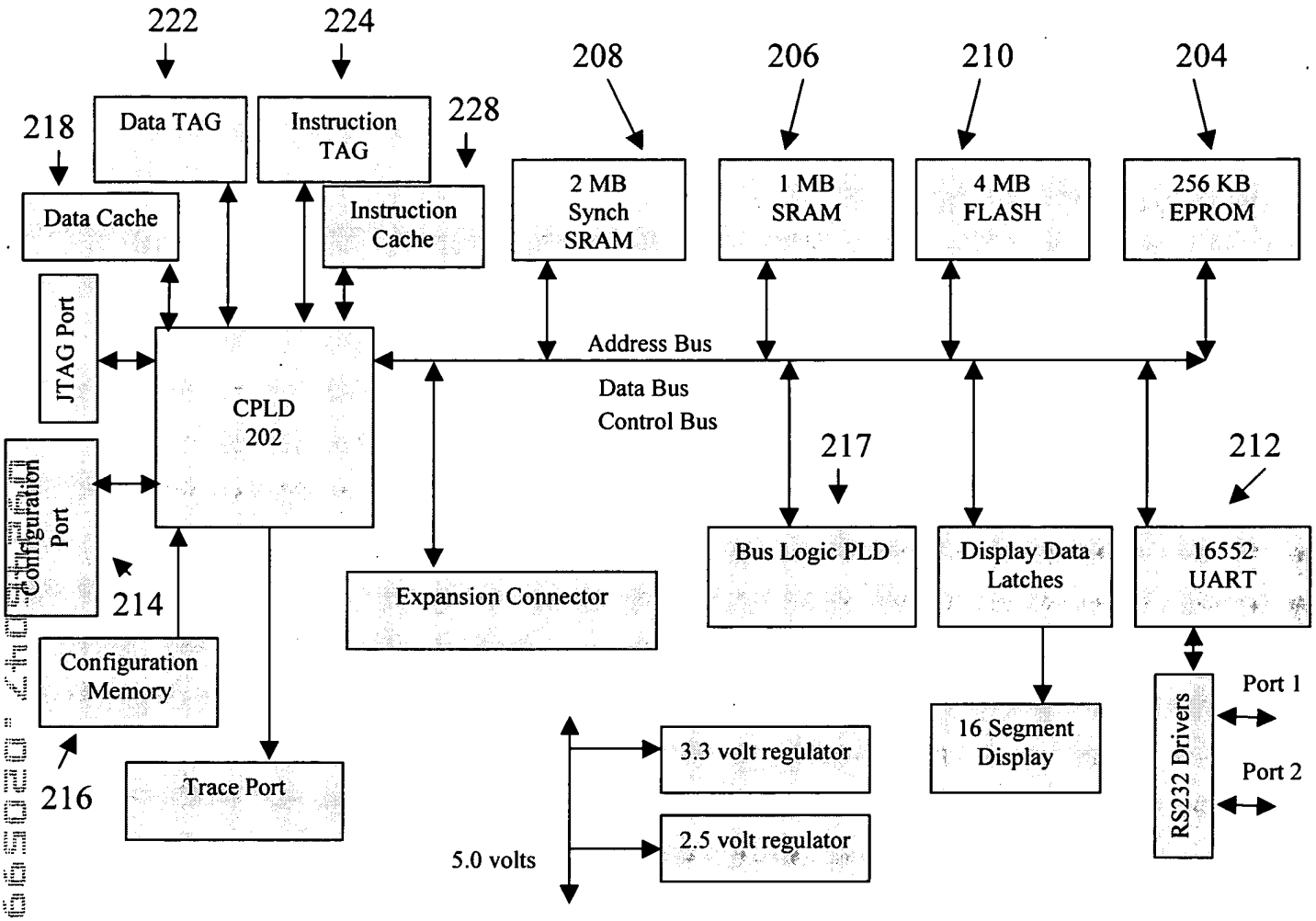

222
224
208
206
210
204
218
Data TAG
Instruction TAG
228
2 MB Synch SRAM
1 MB SRAM
4 MB FLASH
256 KB EPROM
Data Cache
Instruction Cache
JTAG Port
Address Bus
Data Bus
Control Bus
CPLD 202
217
212
Configuration Port
214
Bus Logic PLD
Display Data Latches
16552 UART
Expansion Connector
Configuration Memory
Port 1
Port 2
RS232 Drivers
16 Segment Display
3.3 volt regulator
5.0 volts
2.5 volt regulator
216
Trace Port
200

FIGURE 8

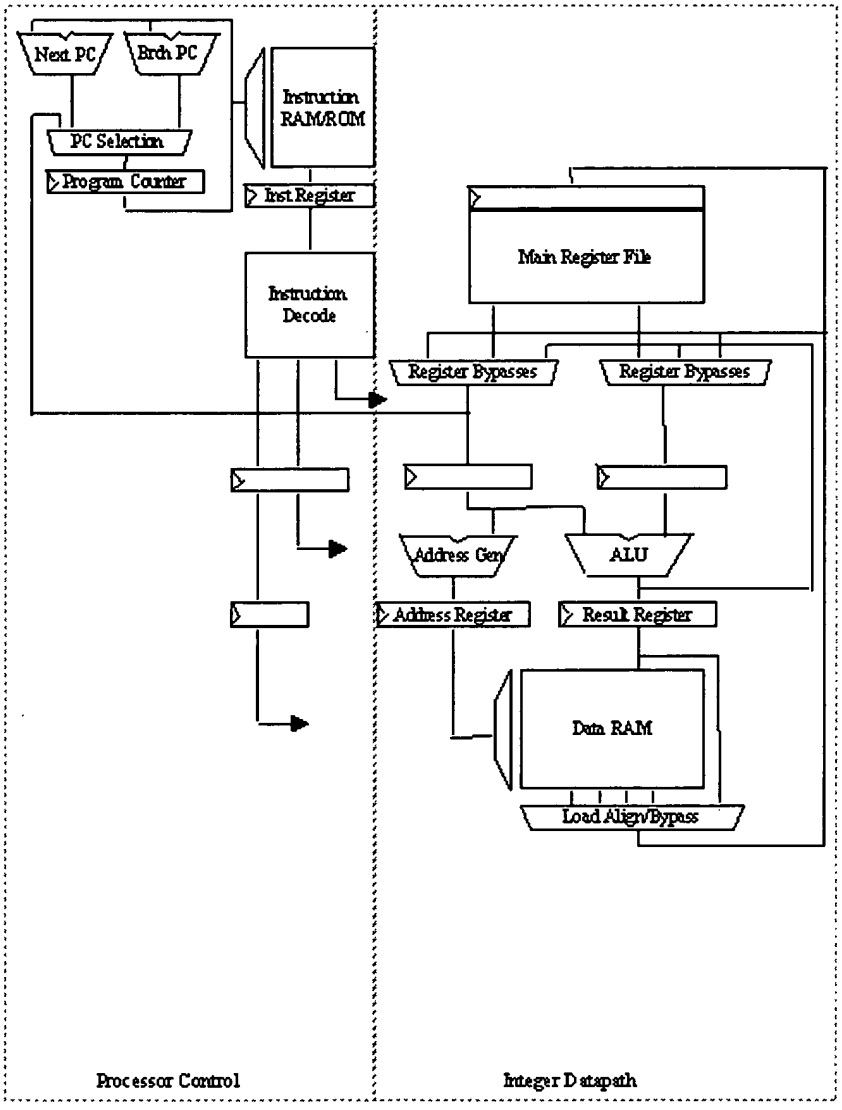

Next PC
Brch PC
PC Selection
Program Counter
Instruction RAM/ROM
Inst Register
Instruction Decode
Main Register File
Register Bypasses
Register Bypasses
Address Gen
ALU
Address Register
Result Register
Data RAM
Load Align/Bypass
Processor Control
Integer Datapath

FIGURE 9

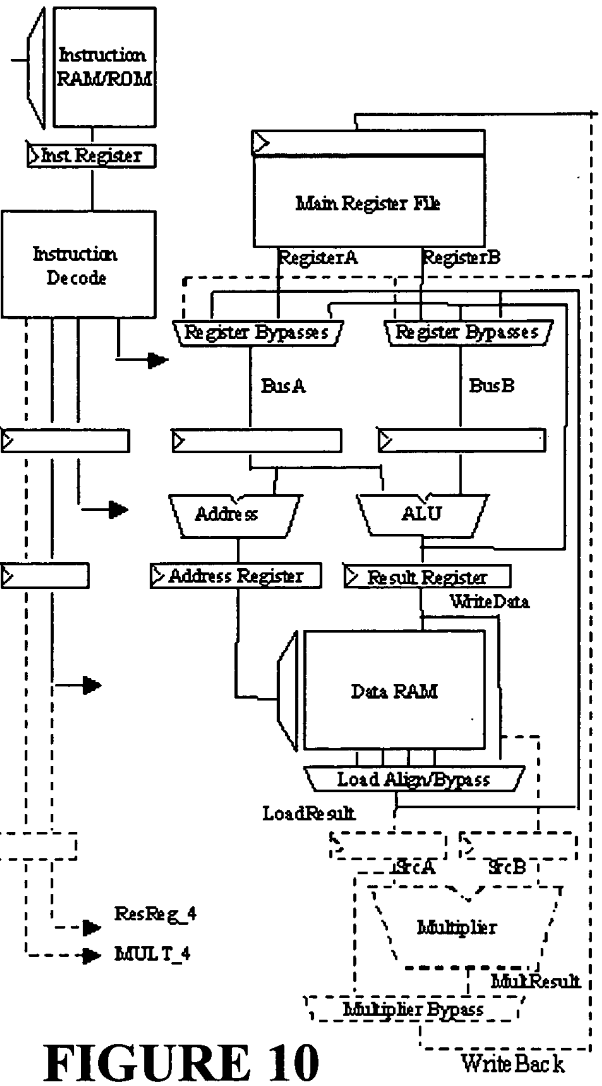

Instruction RAM/ROM
Inst Register
Main Register File
Instruction Decode
RegisterA
RegisterB
Register Bypasses
Register Bypasses
BusA
BusB
Address
ALU
Address Register
Result Register
WriteData
Data RAM
Load Align/Bypass
LoadResult
SrcA
SrcB
Multiplier
MultResult
Multiplier Bypass
ResReg_4
MULT_4
WriteBack

FIGURE 10

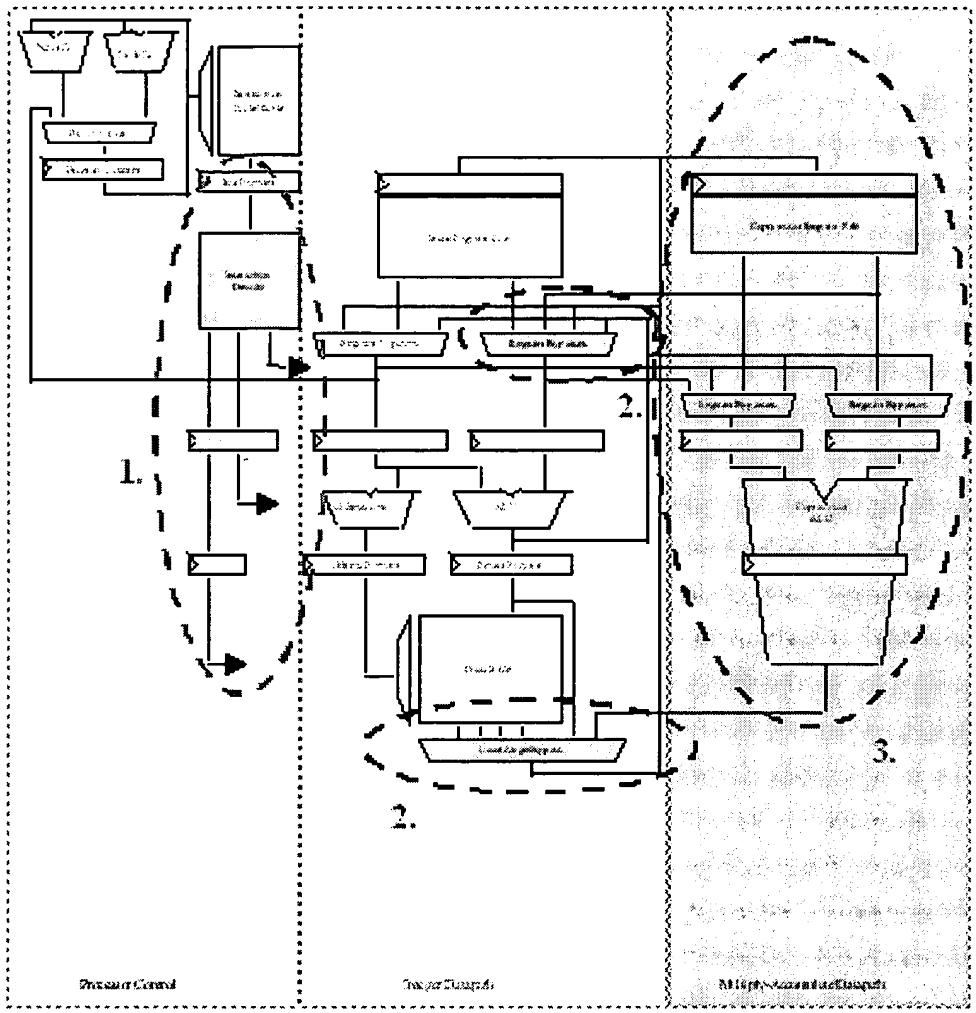


FIGURE 11

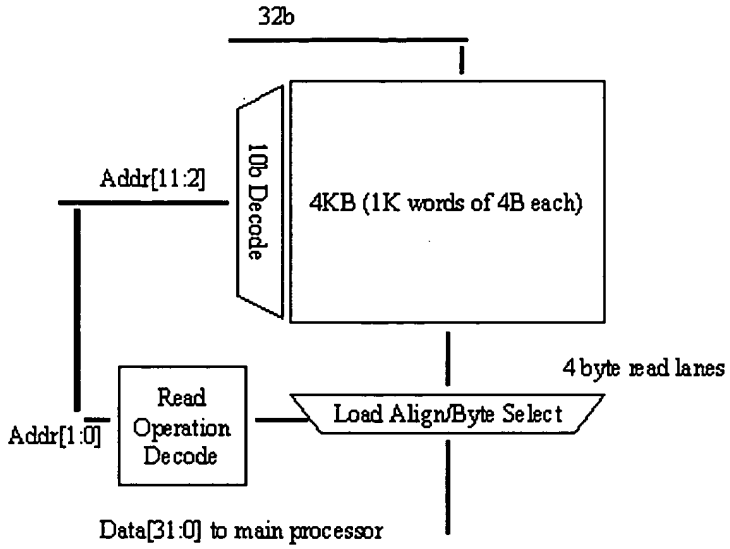


FIGURE 12

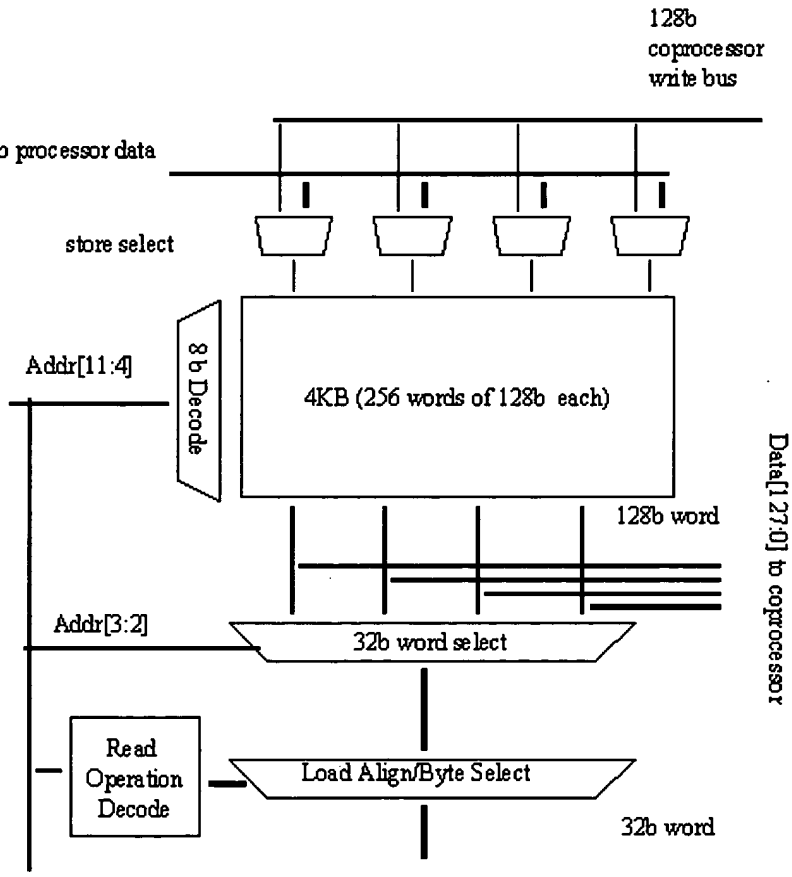


FIGURE 13

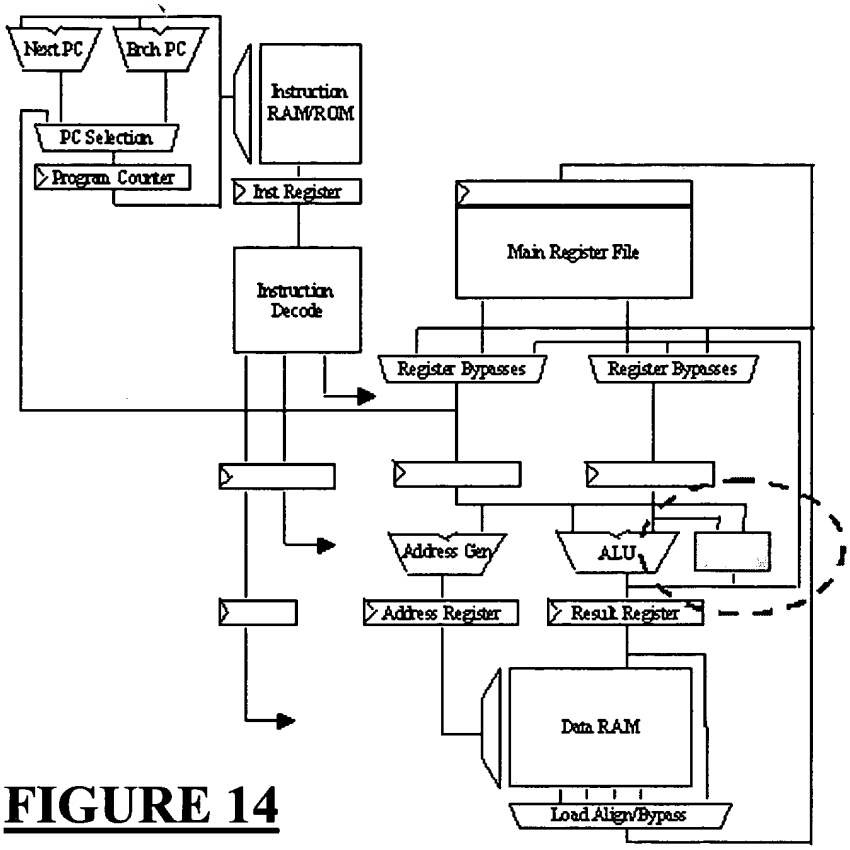


FIGURE 14

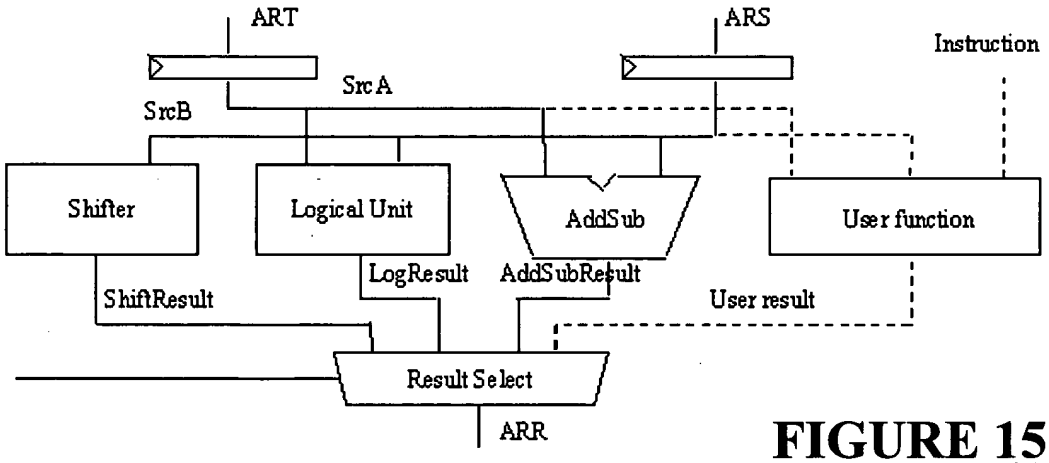


FIGURE 15